



Attorney's Docket No. 42P17989X

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Patent Application of: )

John B. Habert )

Examiner: Michael Thanh Tran

Application No.: 10/749,690 )

Art Unit: 2827

Filed: Dec. 30, 2003 )

Conf. No.: 2187

For: METHOD AND APPARATUS FOR )  
MULTIPLE ROW CACHES PER BANK )

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Respectfully submitted,

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Dated: November 1, 2005

  
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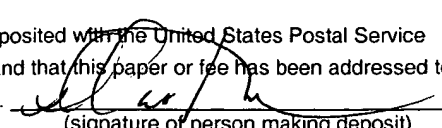
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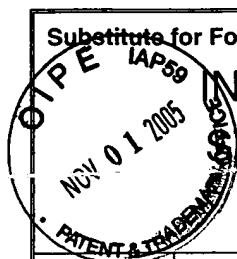
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# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

**Complete if Known**

Application Number	10/749,690
Filing Date	Dec. 30, 2003
First Named Inventor:	John B. Halbert
Art Unit	2827
Examiner Name	Michael Thanh Tran
Attorney Docket Number	42P17989X

Sheet 1 of 2

**U.S. PATENT DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (If known)				
		US-	4,608,666	08/1986	Uchida	
		US-	5,586,294	12/1996	Goodwin et al.	
		US-	5,404,331	04/1995	McClure	
		US-	6,178,479B1	01/2001	Vishin	
		US-	6,330,636B1	12/2001	Bondurant et al.	
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**FOREIGN PATENT DOCUMENTS**

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		Country Code <sup>3</sup>	Number <sup>4</sup>	Kind Code <sup>5</sup> (if known)				
		EP	0 463 617	A2	01/02/1992	Kabushiki Kaisha Toshiba		
		EP	0 704 847	A1	04/03/1996	Kabushiki Kaisha Toshiba		
		PCT/US	2004/043672		04/20/2005	PCT ISR and Written Opinion		

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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> (use as many sheets as necessary)			Application Number	10/749,690
			Filing Date	Dec. 30, 2003
			First Named Inventor:	John B. Halbert
			Art Unit	2827
			Examiner Name	Michael Thanh Tran
			Attorney Docket Number	42P17989X
Sheet	2	of	2	
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		Katsumi Dosaka et al., "A 100-MHz 4-Mb Cache DRAM with Fast Copy-Back Scheme", IEEE Journal of Solid-State Circuits, Vol. 27, No. 11, November 1992, XP 000320439, pages 1534-1538.		

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